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REMARKS

Claims 1-12 were examined in the Office Action mailed March 7, 2006.

Claims 6-12 stand rejected under 35 U.S.C. § 112, 2nd paragraph as indefinite.

Claims 1-3 stand rejected as anticipated by *Mote, Jr.* (U.S. Pat. No. 5,805,609).

Claims 4 and 5 stand rejected as rendered obvious by *Mote, Jr.* in view of IEEE 1149.1 standard, based on a contention that this IEEE standard is analogous art.

Claims 6 and 23 are amended above. Reconsideration of the rejections is respectfully requested in view of these amendments and the remarks which follow.

A. § 112 Rejection of Claims 6-12 is Addressed.

The indefiniteness rejection of claims 6-12 has been addressed by the amendments above to claim 6, wherein the term "respectively" has been added to clarify the connections, consistent with the circuitry shown in Figs. 4-5. Claim 6 has also been amended to correct an informality. No new matter is added thereby. This amendment also addresses the § 112 rejection to claims 7-12, arising from dependency on claim 6.

Claim 12 has been amended to properly conform to Fig. 5.

All of the rejections under 35 U.S.C. § 112 have been addressed specifically, or inferentially by being dependent upon an allowable base claim. Withdrawal of the rejection of claims 6-12 is therefore respectfully requested.

B. § 102(b) Rejection of Claims 1-3 over Mote is Addressed.

The anticipation rejection of claims 1-3 over *Mote* is mooted by the cancellation of claims 1-3.

C. § 103(a) Rejection of Claims 4 and 5 over Mote is Addressed.

The obvious rejection of claims 4 and 5 over *Mote* is mooted by the cancellation of claims 4 and 5.

D. New Claims 13-22 are Presented for Examination.

New claims 13-22 are presented for examination. Support for claims 13-22 is found in an inspection of Figs. 4 and 5, and corresponding specification description, as well as in original claims 6-12. Claim 13 is distinguishable over *Mote* as claiming

a specific boundary scan test circuit topology that is not taught or suggested by Mote, which includes

a first multiplexer circuit for receiving a core logic input signal and a shift/capture control signal;
a capture register circuit coupled to the first multiplexer circuit;
an update register circuit coupled to the capture register circuit;
a second multiplexer circuit coupled to the update register circuit for receiving a mode control signal; and
a buffer coupled to the second multiplexer circuit and to a pad.

Since this combination of features is neither taught nor suggested by Mote, claim 13 (and dependent claims 14-22 which contain these features through dependence from claim 13), are patentably distinguishable over Mote.

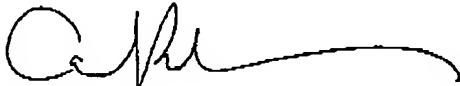
E. Petition for 1-Month Extension.

Applicant hereby petitions for a one-month extension, from June 7, 2006 to July 7, 2006 in which to respond to the Office Action. Please charge Deposit Account No. 50-1123 the \$120.00 large entity 1-month extension fee and any additional fees associated with this transmittal.

F. Conclusion.

In view of the above amendments, claims 6-22 are in form for allowance, and such action is respectfully requested. Should any issues remain, the Examiner is kindly asked to telephone the undersigned.

Respectfully submitted,



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